REMARKS

Claims 1 and 9 are amended. No claims are added or canceled hereby. Accordingly, claims 1-9 remain pending in this application. Support for the amendments to claims 1 and 9 may be found, for example, in the specification at paragraphs [0050], [0067], and [0073].

In the Office Action, the Examiner rejected claims 1-9 under 35 U.S.C. § 103(a) as unpatentable over Reiss et al. (U.S. Patent Application Publication No. 2003/0014145) in view of Fairbairn et al. (U.S. Patent No. 6,625,497). The Applicant respectfully disagrees with the rejection and, therefore, respectfully traverses same.

Claims 1-9 are patentable distinguishable over the combination of Reiss et al. and Fairbairn et al. because they recite a method of operating a semiconductor processing system combining a number of features including, among them, determining first and second states for a wafer via optical digital profiling using critical dimension data and sidewall angle data. Neither Reiss et al. nor Fairbairn et al. describe or suggest the combination recited by claims 1-9. Accordingly, the Applicant respectfully submits that claims 1-9 are patentable thereover.

Reiss et al. describes an integration of fault detection with run-to-run control. As recognized by the Examiner, Reiss et al. does not teach that the first and second states are determined via optical digital profiling.

The Examiner relied on Fairbairn et al. to provide this teaching, which is absent from Reiss et al. The Applicant respectfully disagrees with the combination of Fairbairn et al. with Reiss et al. at least for the reasons set forth below.

Fairbairn et al. discusses the construction and operation of a semiconductor processing module with integrated feedback/feed forward metrology. In particular, Fairbairn et al. addresses:

> the problem of CD control by reducing the CD variation by feeding back information gathered during inspection of the

> wafer (e.g., after photoresist development) to upcoming lots that will be going through the photolithography process, and by feeding forward information to adjust the next process the inspected wafer will undergo (e.g., the etch process).

(Fairbairn et al. at col. 4, lines 40-46.) As discussed by Fairbairn et al., the inspection method employed relies on CD-SEM, which refers to Critical Dimension-Scanning Electron Microscopy. (See, Fairbairn et al. at col. 4, lines 51-60, and at col. 2, lines 24-40.) As those skilled in the art would appreciate, SEM is a destructive (or at least potentially destructive) inspection methodology unlike optical digital profiling, which is non-destructive. Since Fairbairn et al. focuses on a destructive inspection methodology, those skilled in the art would not consider combining Fairbairn et al. with Reiss et al. to arrive at the combination recited by claims 1-9 of the present application. Accordingly, the Applicant respectfully submits that the combination of these references does not render obvious the subject matter of claims 1-9.

The Applicant understands that Fairbairn et al. discusses one other measurement tool other than CD-SEM. In particular, as pointed out by the Examiner, Fairbairn et al. states:

> A CD measurement tool **906**, such as an optical measurement tool utilizing scatterometry or reflectometry techniques, is mounted inside factory interface **905**. An example of a tool that can be used as a measurement tool **906** is imager **310** described above (see FIGS. **3** and **4A**), which can include the CD measurement tool described in U.S. Patent No. 5,963,329.

(Fairbairn et al. at col. 11, lines 21-27.) U.S. Patent No. 5,963,329 (hereinafter Conrad et al.), however, does not describe a method or an apparatus where first and second states for a wafer are determined via optical digital profiling using critical dimension data and sidewall angle data. Accordingly, the mere mention Conrad et al. by Fairbairn et al. cannot be relied upon to provide motivation for one skilled in the art to arrive at the combination recited by claims 1-9.

Conrad et al. discusses a method and apparatus for measuring the profile of small repeating lines. In particular, Conrad et al. emphasizes that the apparatus and method described therein are used to determine the line profile of repeating lines, such as a grid pattern, on a substrate. Conrad et al. states:

> The present invention is a method for nondestructively determining the topographical cross-section of lines on a substrate which provides line thickness, line width, and the shape of the line edge (the line profile). While **a repeating structure, or grating, is required for the measurement**, the method uses broad band illumination, does not involve contact with the substrate and can equally be used for buried planarized gratings. The method takes advantage of available parallel processing computer capabilities for providing rapid line profiles.

(Conrad et al. at col. 4, lines 7-16 (emphasis added).) Accordingly, Conrad et al. does not concern an apparatus or a method where first and second states for a wafer are determined via optical digital profiling using critical dimension data and sidewall angle data. Moreover, those skilled in the art would not look to Conrad et al. to supplement Fairbairn et al. or Reiss et al. to arrive at the present invention. Accordingly, the Applicant respectfully submits that the Examiner has not set forth a rejection that may be sustained. The Applicant respectfully requests, therefore, that the Examiner withdraw the rejection and pass claims 1-9 to issue.

Each of the rejections having been addressed, the Applicant respectfully submits that the claims are now in condition for allowance and a notice to that effect is respectfully requested.

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Respectfully submitted,

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